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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,750	11/15/2002	Cheng-Jye Liu	8711-US-PA	7526

31561 7590 01/12/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
LUU, CHUONG A	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,750	LIU ET AL.	
	Examiner	Art Unit	
	Chuong A Luu	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-21* is/are allowed.

6)☒ Claim(s) *1-6 and 8-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 1-6 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kluth et al. (U.S. 6,376,341 B1) in view of Wolf et al. (Silicon Processing).

Kluth discloses a method for fabricating a memory cell with

(1) forming a silicon oxide (26)/silicon nitride (28)/silicon oxide (30) (ONO) stacked layer (24) on a substrate (23), the ONO stacked layer (24) consisting of a bottom oxide layer (26), a silicon nitride layer (28) and a top oxide layer (30);

forming a masking layer (protective layer) (36) on the ONO stacked layer (24);

patterning the masking layer (protective layer) (36) and the ONO stacked layer (24) to form a plurality of stacked patterns (see Figure 6);

removing the masking layer (protective layer) (36), which becomes layer (34) (see column 6, lines 66-67);

(3) wherein a thickness of the bottom oxide layer is about 50-150 Å (50-100 Å) (see column 5, lines 28-29);

(4) wherein a thickness of the silicon nitride layer is about 50-200 Å (55-80 Å) (see column 5, lines 35-43);

(5) wherein a thickness of the top oxide layer is about 50-150 Å (70-120 Å) (see column 5, lines 44-46);

(6) the the masking layer (protective layer) (36) comprises silicon nitride (see column 5, lines 49-50);

(9) wherein the ONO stacked layer (24) is patterned until a portion of the bottom oxide layer (26) is exposed "on the sidewall" (see Figure 6);

(10) wherein the exposed bottom oxide layer (26) is removed after the ion implantation is performed (see Figures 3-5);

(11) wherein the insulator comprises silicon oxide (50) (see column 6, line 67).

Kluth discloses the claimed invention except for wherein an etching rate of the protective layer is lower than an etching rate of the top oxide layer; wherein removing the protective layer comprises using wet etching to remove the protective layer; and specific thicknesses of ONO layer. However, Wolf discloses silicon processing for the VLSI ERA with **(1)....** wherein an etching rate of the protective layer is lower than an etching rate of the top oxide layer (see pages 532-534); **(2)** wherein removing the protective layer comprises using wet etching to remove the protective layer (see pages 532-534). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the etching rate of protective layer and the

oxide layer of Kluth's device (accordance with the teaching of Wolf) within the range as claimed for the purpose of obtaining the better arrangement of the optical signal transmission elements and reduce the insertion loss, and it also has been held that where the general conditions of a claim are disclosed in the prior ad, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. In re Aller, 105 USPQ 233 (see MPEP 2144.05).

Claims 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kluth et al. (U.S. 6,376,341 B1) in view of Wolf et al. (Silicon Processing) and further in view of Randolph et al. (U.S. 6,538,270 B1).

Kluth and Wolf disclose everything above except for forming a plurality of word lines on the substrate; wherein the word lines comprise polysilicon. Furthermore, Randolph discloses an array of memory cell with **(8)** further comprising:..... forming a plurality of control gate electrode (228) (word lines) on the substrate (see column 4, lines 24-29. Figure 6); **(12)** wherein the control gate electrode (228) (word lines) comprise polysilicon (see column 4, lines 26-27). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the teachings of Kluth and Wolf (accordance with the teaching of Randolph). Doing so would facilitate the manufacture of the semiconductor device and increase the connectivity and the life of the memory cell.

Allowable Subject Matter

Claims 13-21 are allowed.

The following is an examiner's statement of reasons for allowance: The examiner has reviewed the prior art in light of applicant's claimed invention and finds that the combined limitations claims define over the prior art.

Response to Arguments

Applicant's arguments filed October 5, 2004 have been fully considered but they are not persuasive.

Applicant argues that Kluth not only fails to provide requisite suggestion or motivation of, but rather teach away from the recited limitation of forming the protective layer in a thickness of 50Å. Kluth does not explicitly disclose thickness of the protective layer of 50Å. However, the thickness of the protective layer of 50Å being within the range 50 Å is considered to be obvious. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the etching rate of protective layer and the oxide layer of Kluth's device (accordance with the teaching of Wolf) within the range as claimed for the purpose of obtaining the better arrangement of the optical signal transmission elements and reduce the insertion loss, and it also has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. In re Aller, 105 USPQ 233 (see MPEP 2144.05).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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December 27, 2004

CARIDAD EVERHART
PRIMARY EXAMINER